Development of a Timing and Data Link for EIC Common Hardware Platform

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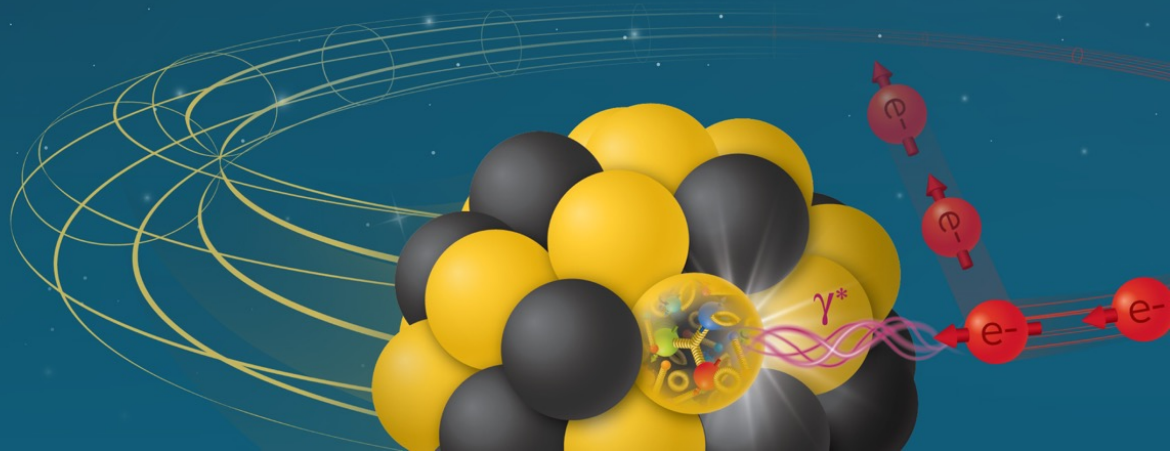
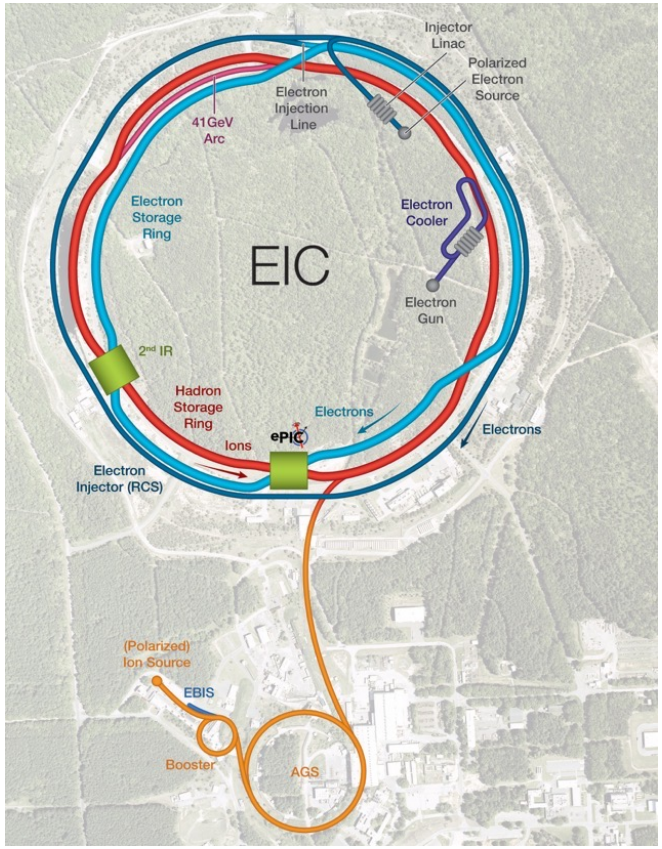
October 23rd, 2023



Electron-Ion Collider

EIC Project Overview

- Upgrade to RHIC
  - Hadron Storage Ring
  - Electron Storage Ring
  - Rapid Cycling Synchrotron
- Subsystems
  - Electron Gun
  - Electron Cooler
  - Injector Linac
  - Electron Beam Ion Source
- Existing Systems
  - Linac
  - Booster
  - AGS



RHIC Timing Links

- Low Level RF Update Link
  - RF system event and data distribution
  - Supports bidirectional data transfer
- Event Link
  - Broadcasts 8-bit event codes
- Real Time Data Link
  - Distributes timestamp data
- Beam Synchronous Link
  - Carrier synchronous to the machine revolution frequency
- Accelerator Master Clock Signal
  - RF clock distributed to systems

Timing Data Link Goals

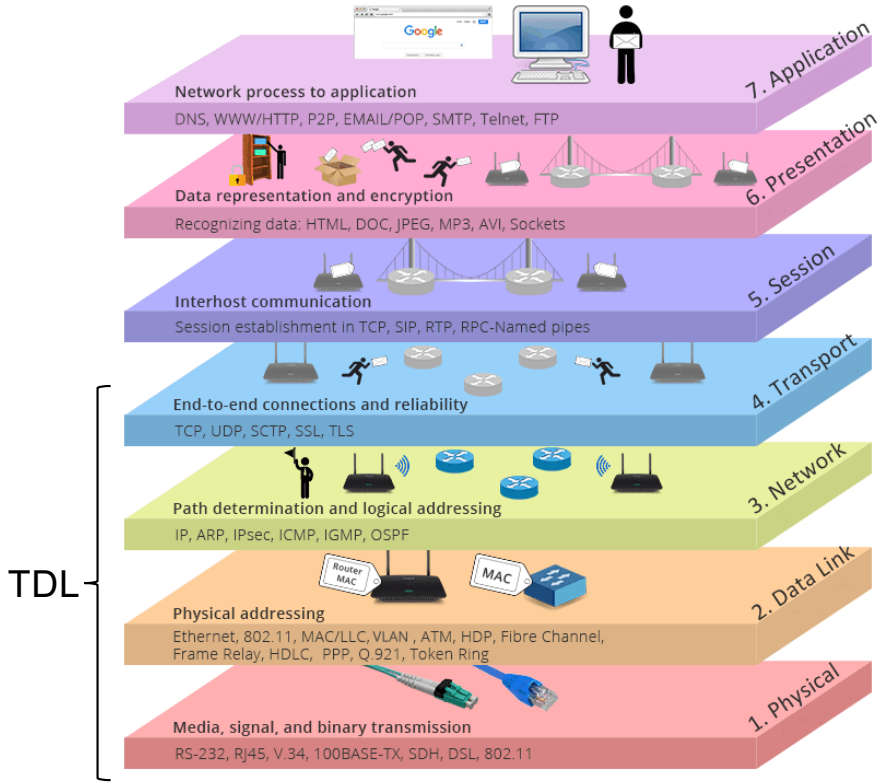
- Consolidate existing timing links
- Deterministic distribution of critical timing data
- Distribution of Accelerator Master Clock
- Packet filtering based on event ID and data
- Bidirectional data transfer for distributed feedback
- Modular and configurable
- Scalable to meet the needs of the large machine and various subsystems
- EIC first run planned for 2031
  - Must have verified prototype hardware by Q1 2024 for Technical Review

Timing Data Link Requirements

- Synchronized timestamps with 1ns resolution
- RF clock distribution with < 10ps rms additive phase jitter
- Data throughput of 6.4 Gbps on each link
- Able to support an arbitrarily large number of network endpoints
- Automatic link latency compensation
- Distribution of beam diagnostic data
  - Beam position/loss monitors
  - Beam synchronous events
- Distribution of machine critical information
  - Master permit link
  - Machine protection statuses
  - Subsystem permit signals

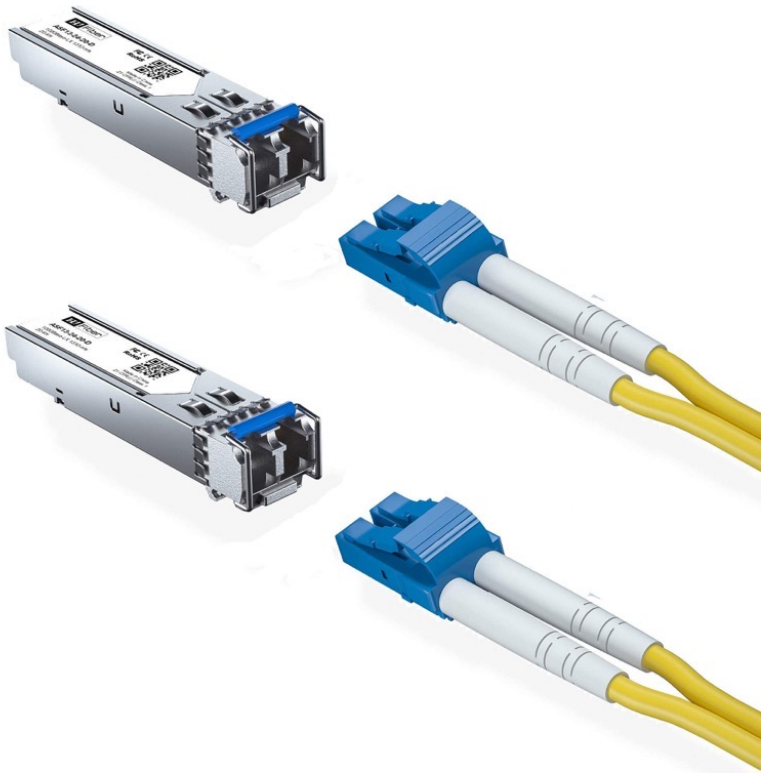
Timing Data Link Specification

- Custom networking protocol
- Defines Layers 1-4 of the OSI model
  - Physical Layer
    - Cables
    - Electrical signaling
    - Symbol encoding
  - Datalink Layer
    - Data word framing
    - Clock synchronization
  - Network Layer
    - Packet routing and filtering
    - Network topology
  - Transport Layer
    - Reliable timestamping
    - Event and data synchronization



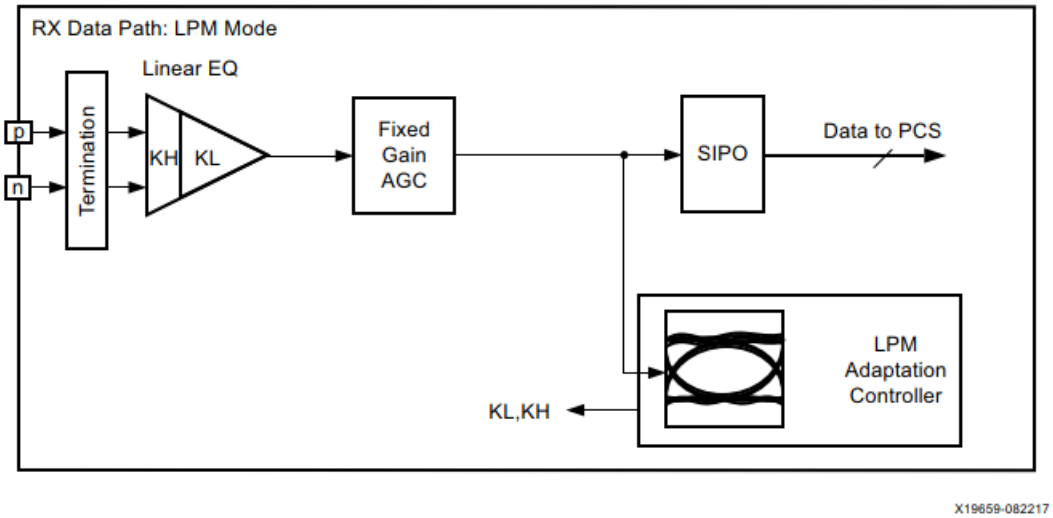
Physical Layer

- Transfers data bytes across the physical medium
- Single-mode or Multi-mode fiber
- SFP+ modular transceivers
- Electrical CML data pairs for TX/RX
- Line rate 8 Gbps
  - Synchronous to 100 MHz Accelerator Master Oscillator
  - Receiver recovers clock
- Encodes bytes into 8b/10b symbols
- Bytes transferred at 800 MB/s



Physical Layer

- Xilinx GTH/GTY transceiver front end with DFE disabled
  - Enable at startup
  - Read stable equalization values via DRP
  - Disable DFE (AGC)
  - Write previously read equalization values
- This allows for good BER
  - Find the center of the eye
- Reduces jitter to acceptable levels (less than 10ps rms)
- Recovered clock can then be forwarded to RF system or jitter attenuator for more cleaning up

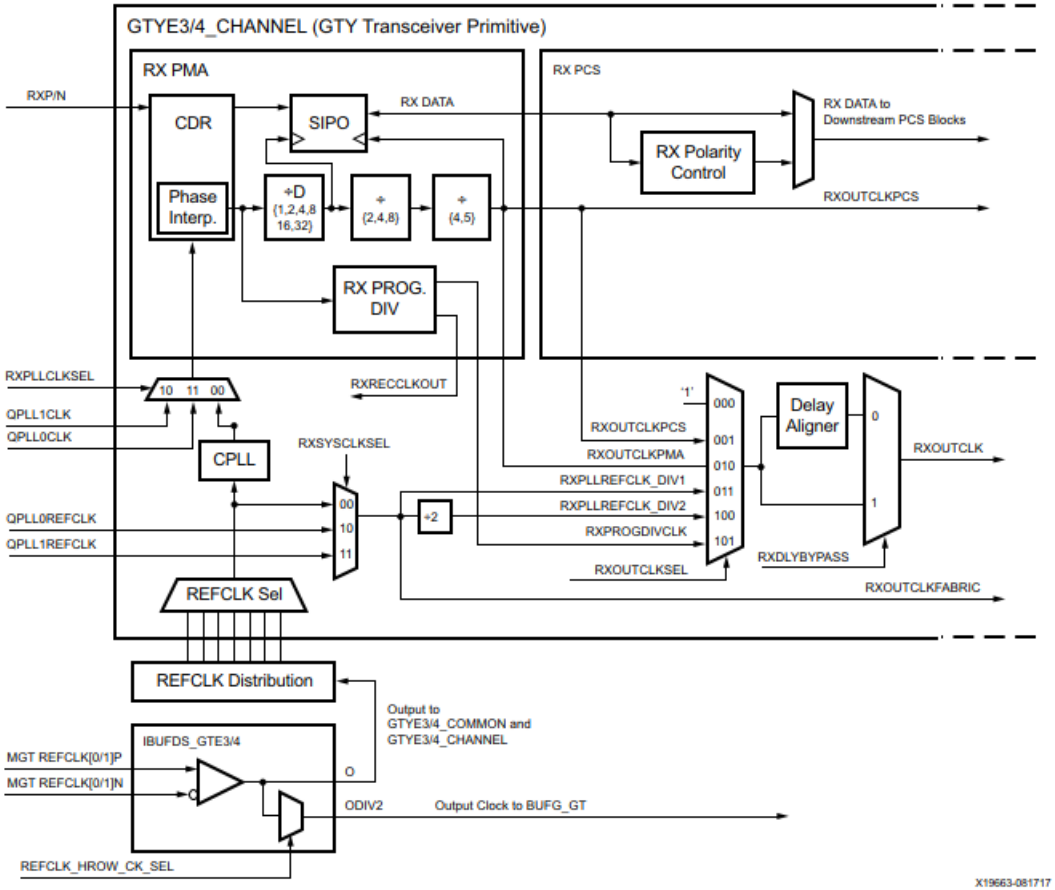


Datalink Layer

- Transfers 64-bit data words between devices
  - Big endian format
- Comma detection to algin words
  - Comma in least significant byte
- Word alignment provides 100 MHz recovered clock synchronization
  - Not trivial
- No addressing is implemented
  - Words are transmitted point to point between linked systems
- Out of band signaling
  - K-symbols
  - Link latency measurement

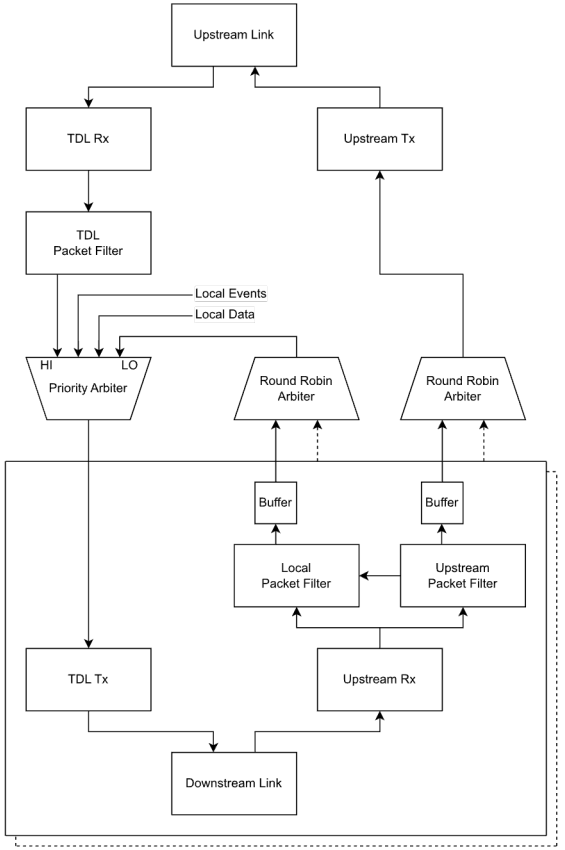
Clock Recovery Phase Alignment

- RX SIPO input is actually a dual edge sensitive flip flop
- Can lock to bit clock on either edge on power up
- User can PMA shift RX clock using bitslip but stuck on whatever edge CDR is locked to
- Disable elastic buffer
- Must “reset-roulette” to catch desired edge for clock synchronization
- RXRECCLKOUT provides -120dB of additive phase jitter
  - Connect to TX user clock for link forwarding



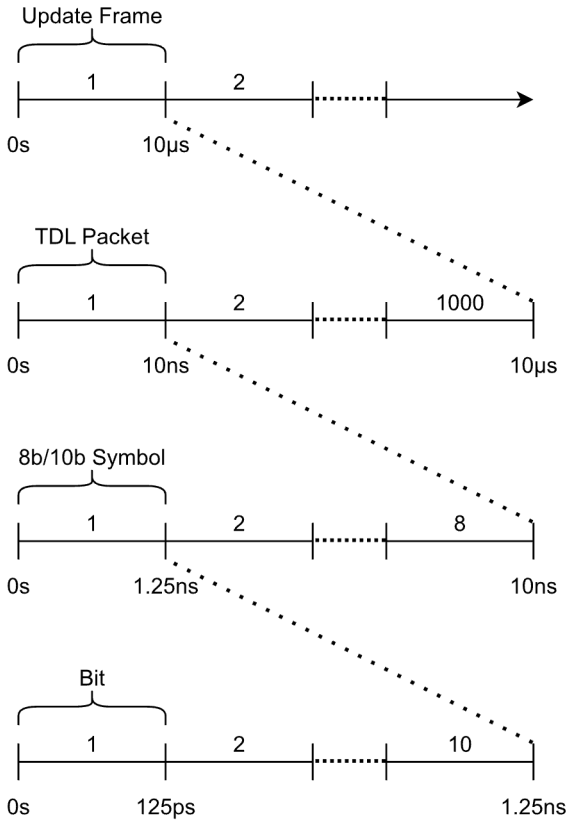
Network Layer

- Routes 64-bit TDL packets between devices
  - 16-bit packet ID and 48-bit data field
- Network follows a tree structure
- Data fields encode special packet and event IDs
- Deterministic packet transmission when traversing the tree in the downstream direction
- Upstream data transmission supported but without guaranteed deterministic timing
- Timing Data Generators broadcast events and data
  - Root node is the Global Timing Data Generator
  - Downstream Timing Data Generators rebroadcast and filter
  - Leaf node devices send data to Upstream Timing Data Generators



Transport Layer

- Update Frames transmitted at 10µs intervals
  - Followed by a timestamp packet
- Update Frame contains 1000 TDL packet
  - Frames begin with Update Event followed by Timestamp packet
  - At least two idle frames to support byte and word alignment
- Data received during an Update Frame is acted upon when the Update Event arrives to synchronize event and data timing
- Timestamp is encoded with a special packet ID
  - 31-bit seconds field
    - Counts seconds since epoch
    - Allows for a 68-year timespan before rollover
  - 17-bit ticks field
    - Counts 10 us ticks (100,000 ticks per second)

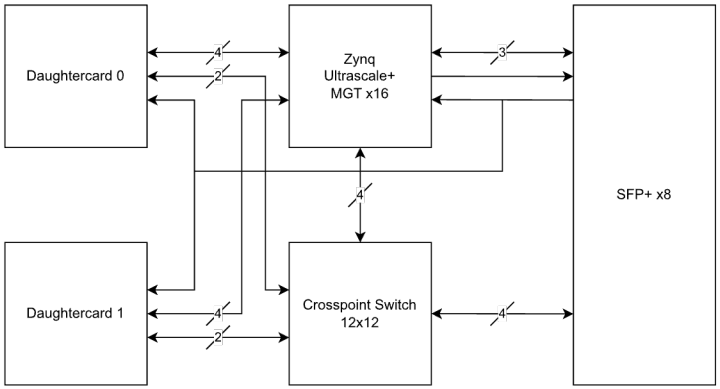


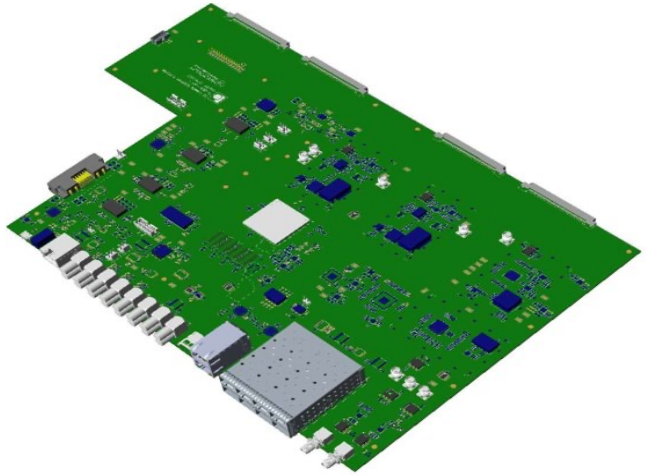
Hardware Implementation

- The EIC Common Hardware Platform
- Carrier Board 2U Chassis
- Modular design with two pluggable daughtercards
- Configurable datapaths for TDL
- Xilinx Ultrascale+ MGTs interface with SFP+
- FPGA handles packet routing and filtering logic
- SFP+ TDL networking daughtercard
- Other special function daughtercards
  - Baseband ADC/DAC
  - RF ADC/DAC
  - Digital I/O

Common Hardware Platform Carrier

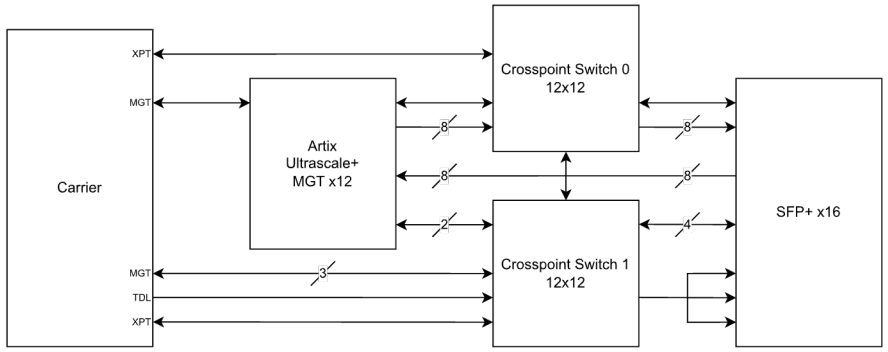
- Provides power and clocks to daughtercards
- Clock sources
  - Analog PLL
  - Digital PLL
  - Beam Synchronous
  - External
- SFP+ x8 one for TDL fanout
- Zynq Ultrascale+ with 16 GTH transceivers
- Crosspoint switch 12x12
- Two daughtercard sites each with
  - Four transceiver lanes
  - Two crosspoint switch lanes
  - Chip-to-chip high speed serial bus

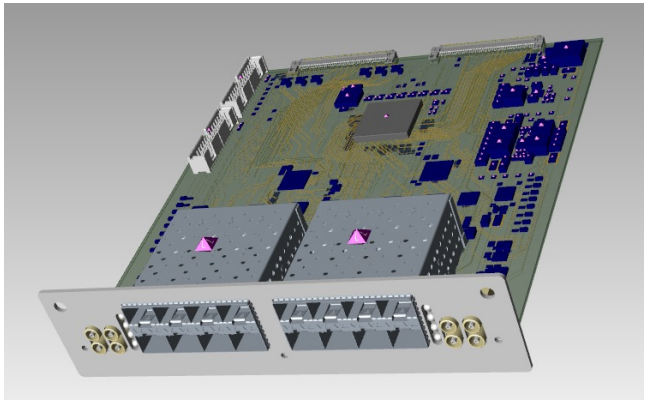




Common Hardware Platform SFP+ Daughtercard

- Mates with CHP carrier
- Provides 16 SFP+ ports
  - 13 bidirectional
  - 3 transmit only for TDL fanout
- Two 12x12 crosspoint switches
  - Highly configurable datapaths
- Artix Ultrascale+ FPGA with 12 GTY transceivers
- One transceiver lane dedicated to chip-to-chip link to carrier
- FPGA will host packet routing and filtering logic

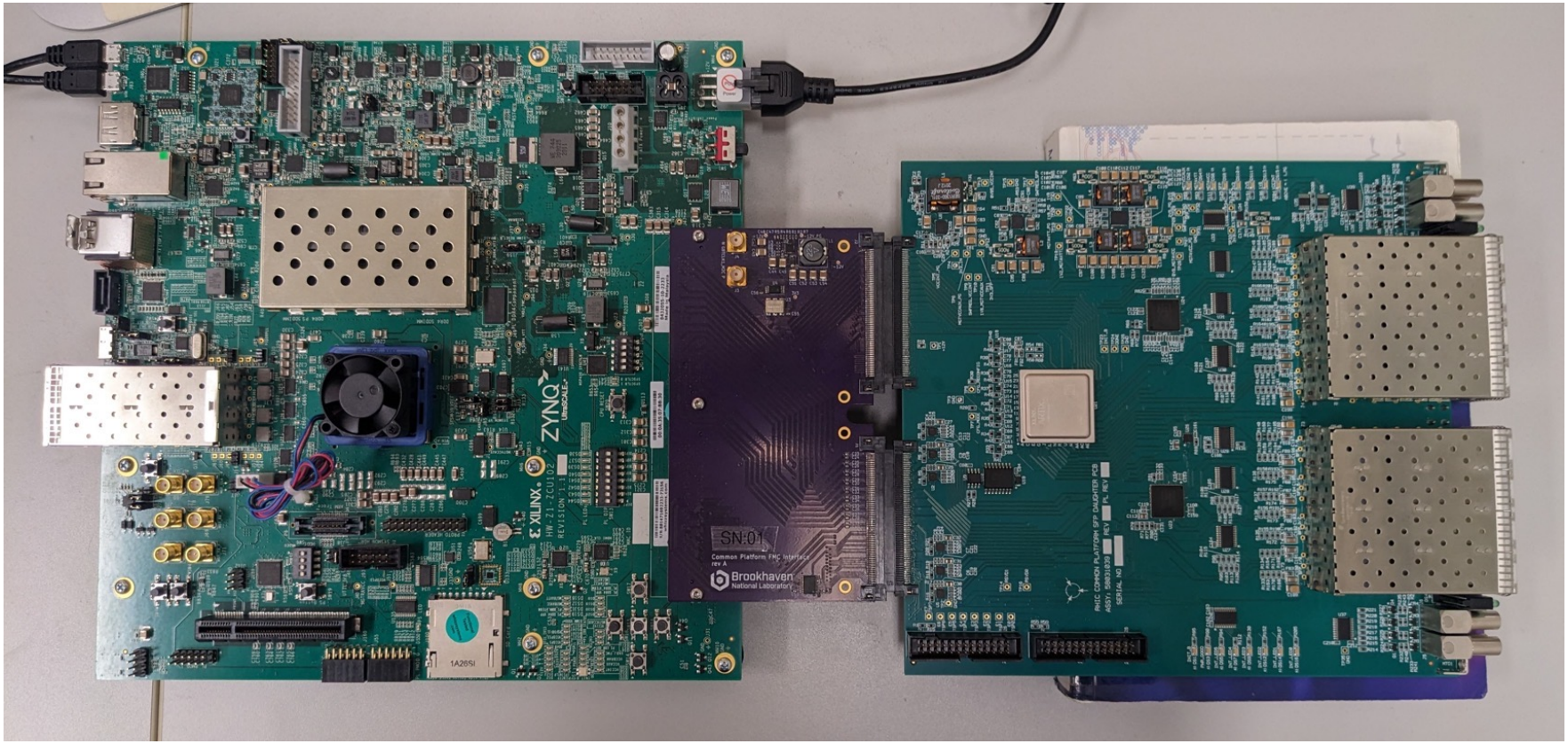




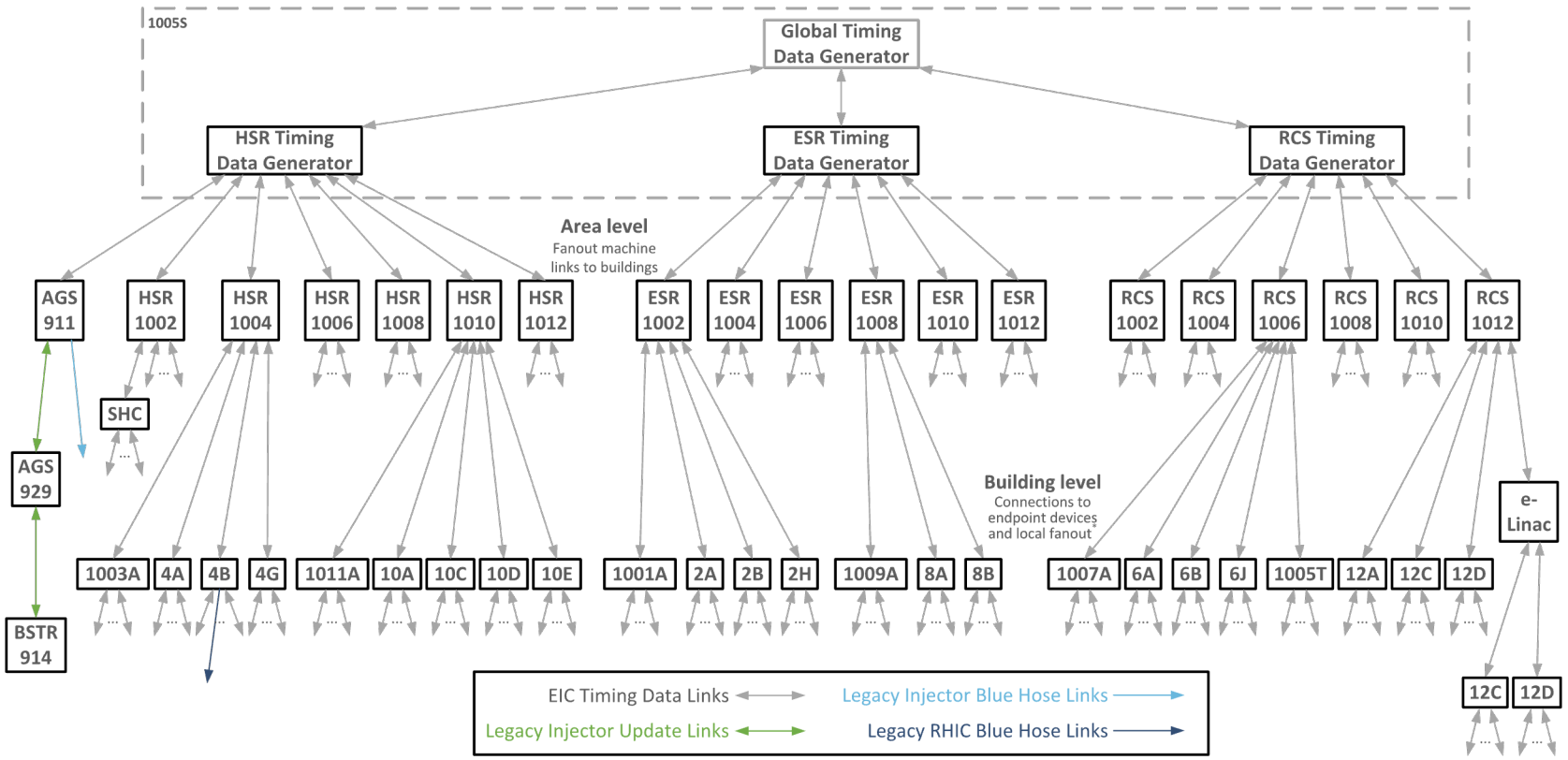
Timing Data Generator

- CHP carrier chassis with SFP+ daughtercards
  - Can have two, one, or even no SFP+ daughtercards
  - Can mix with other special function daughtercards
- Global TDG is the root node of the tree network
  - Transmits Update Frames and Timestamp Packets
  - Global timing events and data
  - Support for periodic event generation 1Hz, 10Hz, 720Hz, etc.
- Downstream TDG are subtree nodes
  - Local timing events and data
  - Packet routing and filtering
  - Upstream link aggregation
- Endpoint devices are leaf nodes
  - Can generate feedback data and send upstream
  - Receive TDL and recover Accelerator Master Clock

Test Setup



EIC TDL Network Diagram



Project Status

- Common Hardware Platform mechanical mockup chassis and PCBs have been fabricated and verified
  - Resistive load boards used to test heat dissipation
  - Fans included to demonstrate airflow
- First prototypes of CHP carrier board PCBs received
  - Currently being tested
- First prototypes of SFP+ daughtercard PCBs received
  - Currently being tested
  - Working Timing Data Link clock recovery demonstrated with eval board as link generator
- Initial testing plan
  - Signal integrity check on high speed links
  - Simple loopback test with TDL protocol
  - Communication between devices
  - Integration testing in a tree network